



Design Platform

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Chips for Europe
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Design in the semiconductor value chain

50%

added value of design across the value chain

BCG/SIA

fabless **growth** in 10 years **+170%**

IBS

35%

fabless revenue **share** of total IC

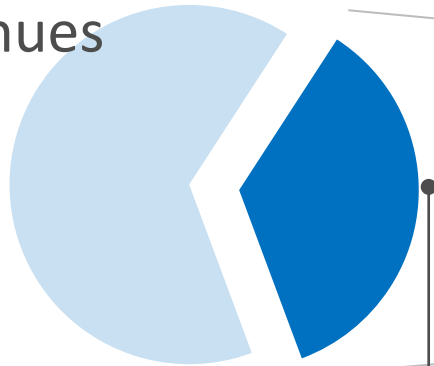
IC Insights
market

Europe's fabless problem

8%

Europe's **share** of design revenues
Mostly in lower added-value
designs

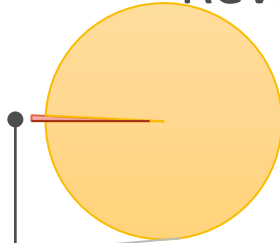
IC Market
Revenues



35%

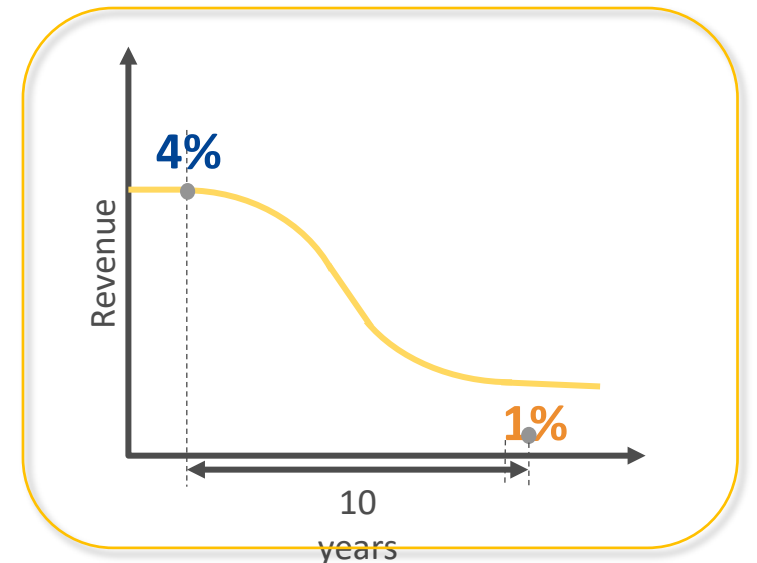
Fabless

Fabless
Revenues



<1%

Europe

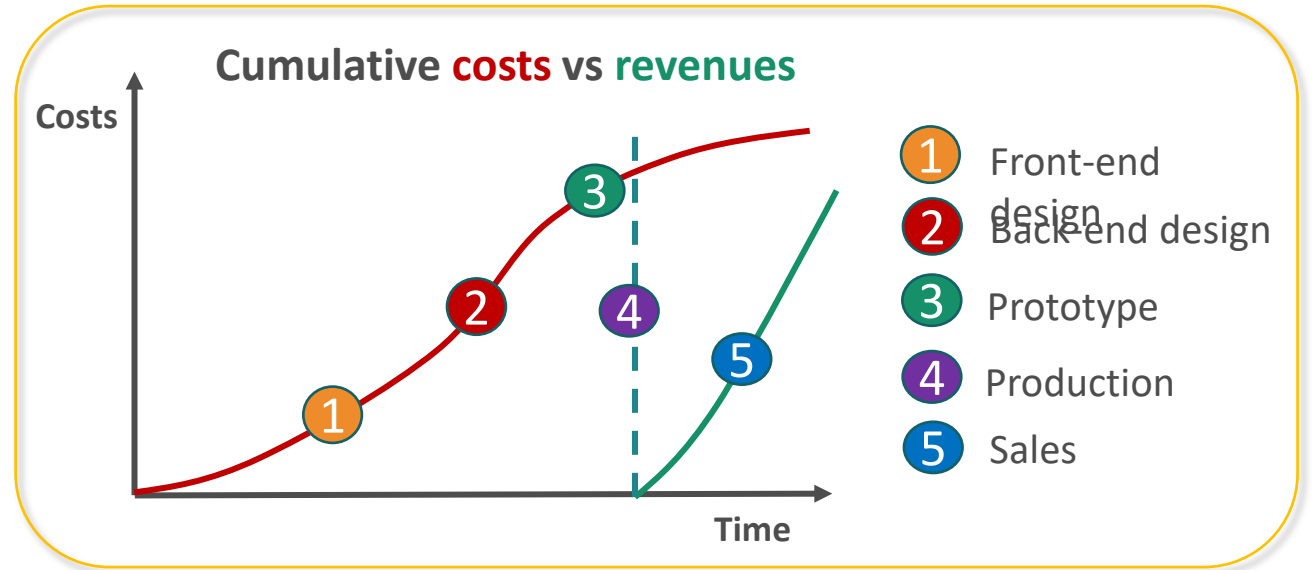
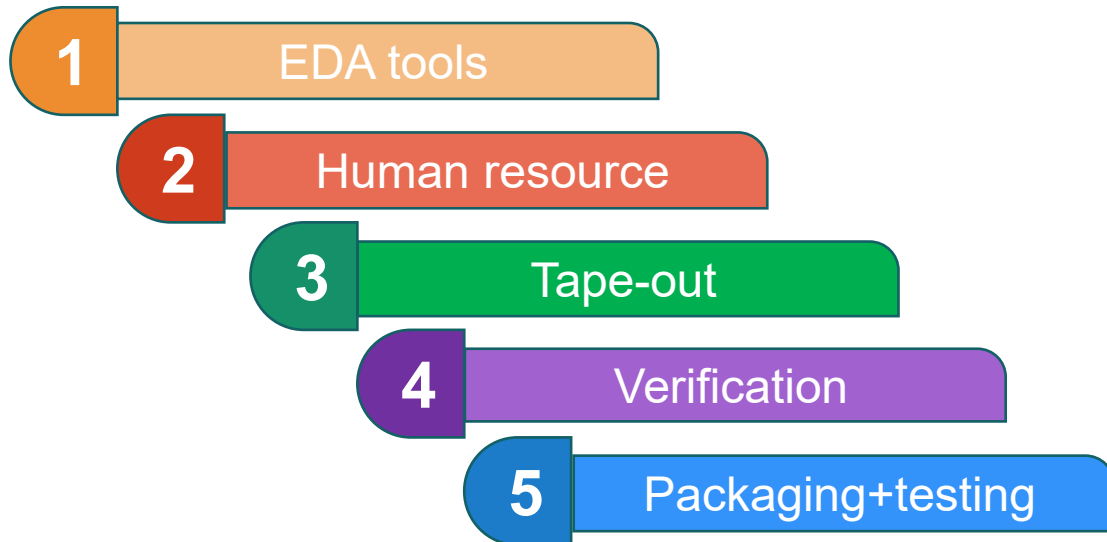


Share of **fabless** declined in
10y

Source: IDC, IC Insights

Challenges for fabless companies

Main costs as from user poll:



Costs paid to 3rd parties:

1. Licensing: EDA, IP, PDK
2. Fabrication: MPW, Masks, Package, Test
3. IT/infra: CapEx + maintenance, or cloud

GOAL: faster and cheaper design process for SMEs!

Design platform - scope



Main objectives

- **Reduce entry barriers** and admin burden for EU companies in design
- **Facilitate access** to pilot lines and foundries
- Foster **collaboration** among EU stakeholders on new developments



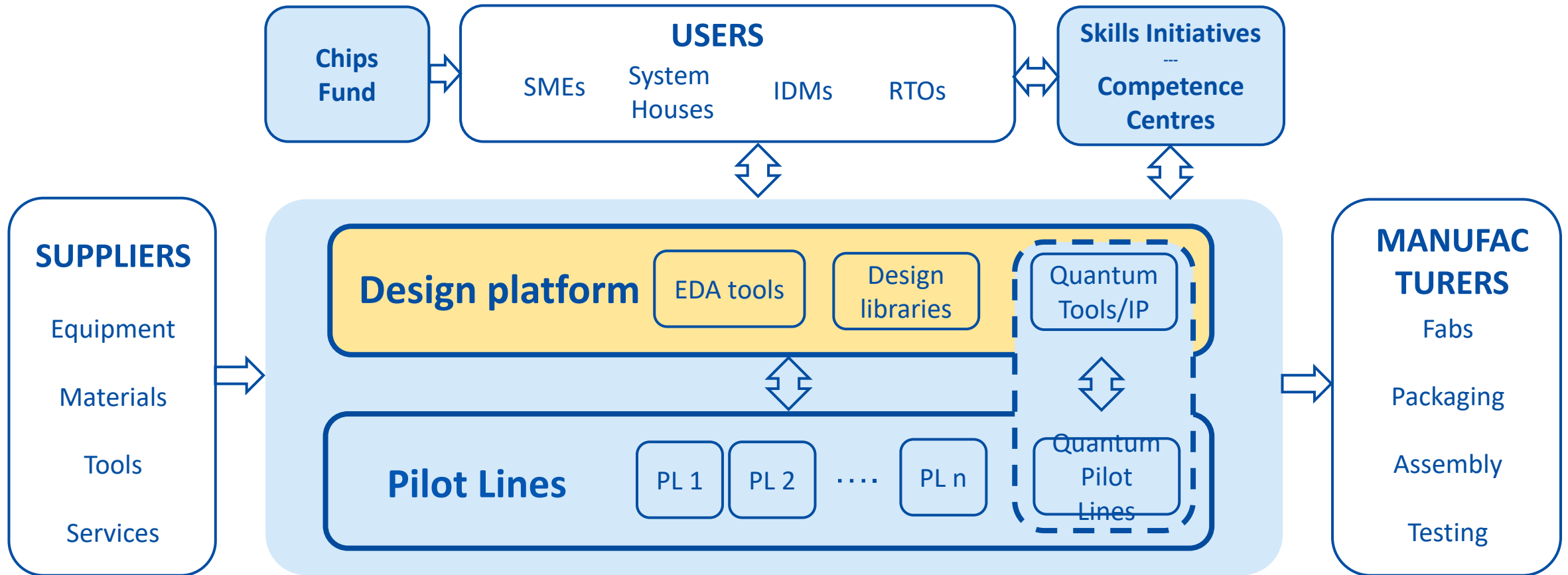
Instrument **ning** and support to boost design skills



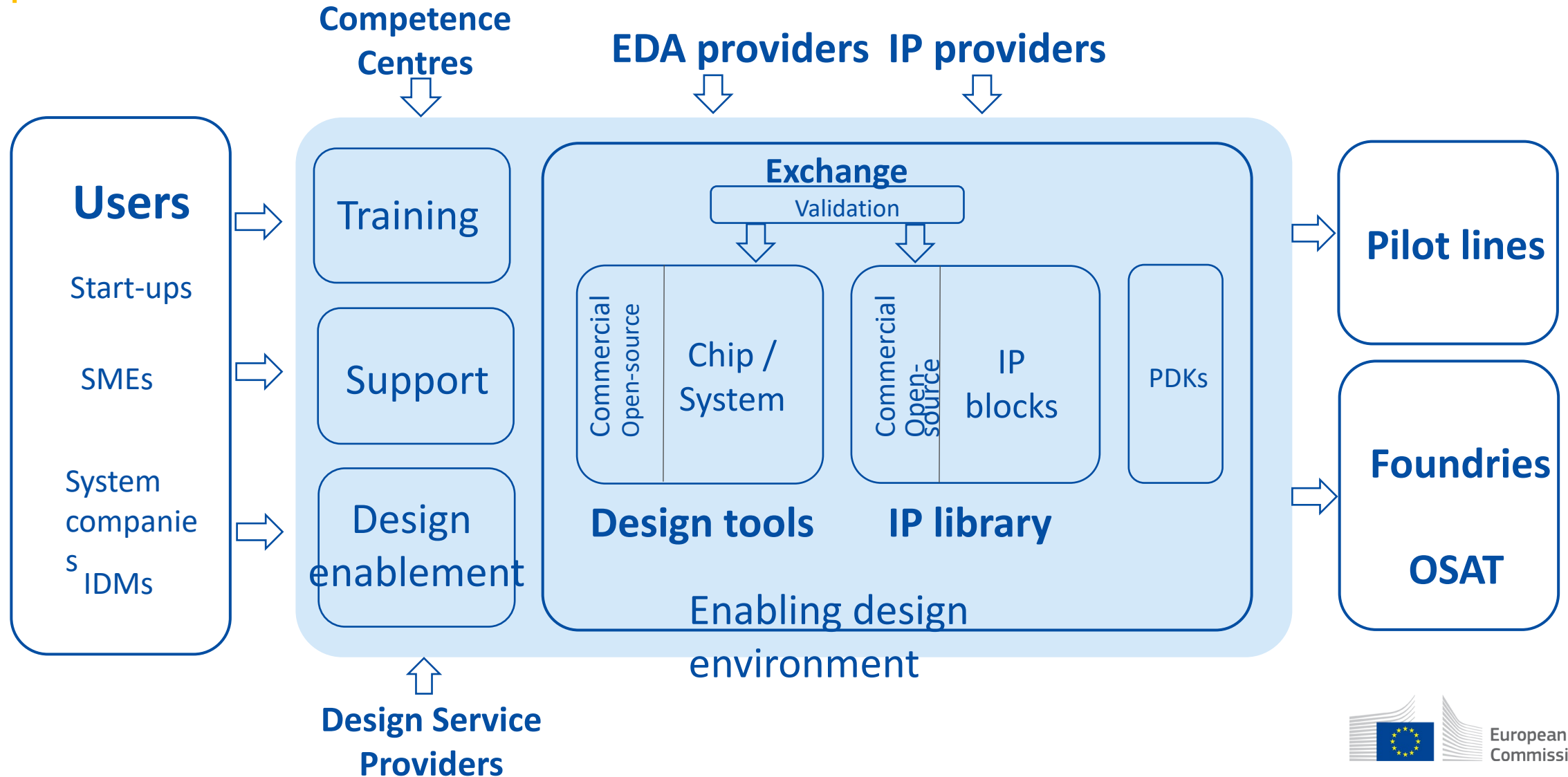
Develop a **virtual design platform**, offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

Chips for Europe Initiative

Central role of Design Platform



Design platform

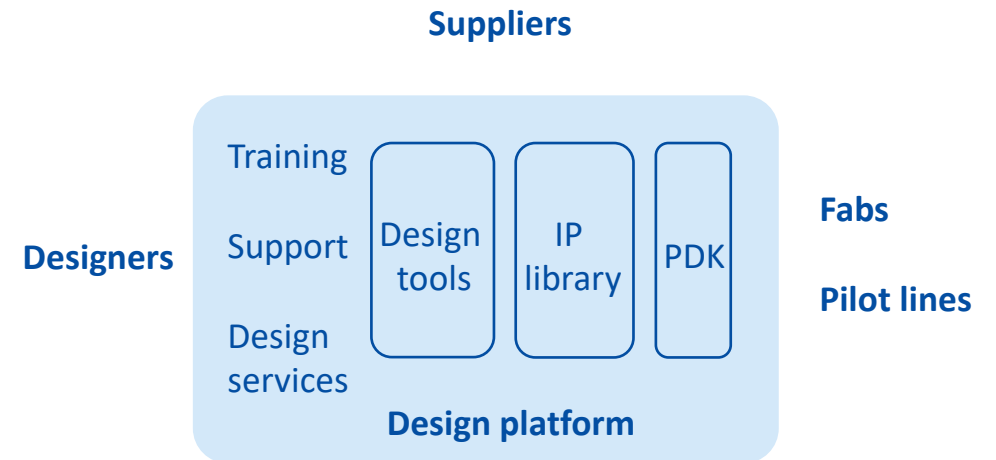


Design platform – added value



User benefits

- Easy access to **tools and IP** in a **secure, scalable** cloud environment
- **Streamlined** licensing process
- **Enablement** support up to tape-out
- Collaborative spaces for new developments
- Training and support



Design platform - cloud



Why cloud?



- No upfront CapEx for on-premise IT



- Maximum computing **scalability**



- Growing trend due to increased **efficiency** and **flexibility**



- **AI/ML** integration in design: game-changer

Design Platform Implementation

Design Platform Working Group

Ansys

APPLIED MATERIALS®

arm

cādence

codasip®

DASSAULT SYSTEMES

DOLPHIN DESIGN

Fraunhofer

infineon

imec

Racyics

SIPEARL

SIEMENS

ST

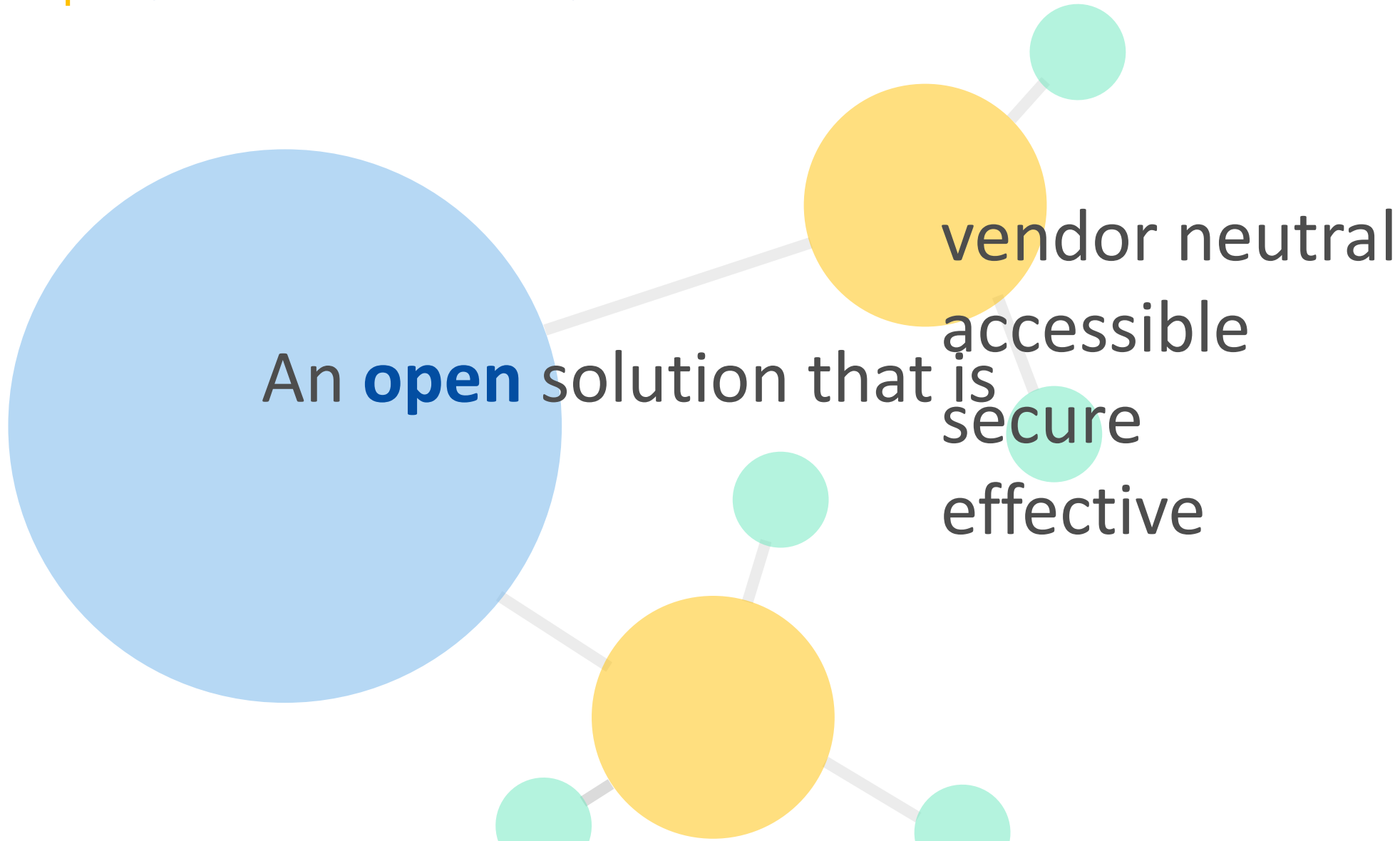
SYNOPSYS®

wide coalition of EDA tools & IP vendors, RTOs, IDMs, design houses,

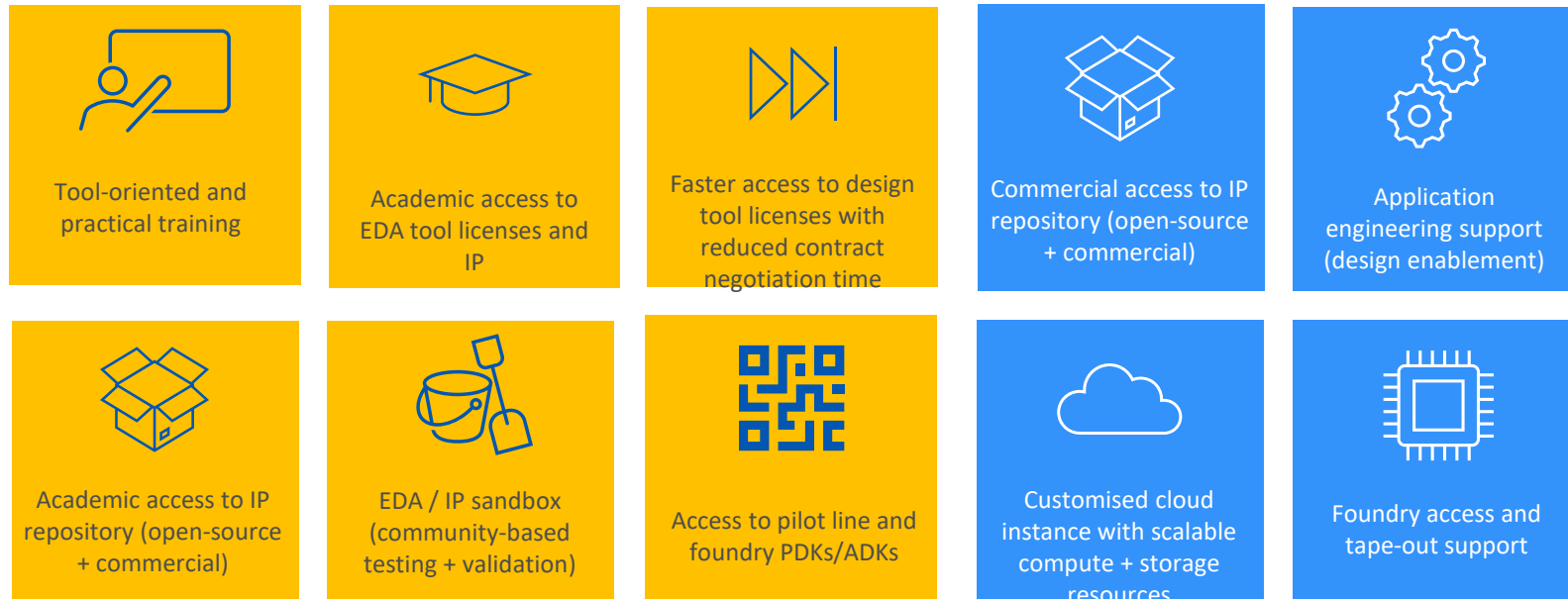
common aim: strengthening Europe's design ecosystem

Design Platform Working Group

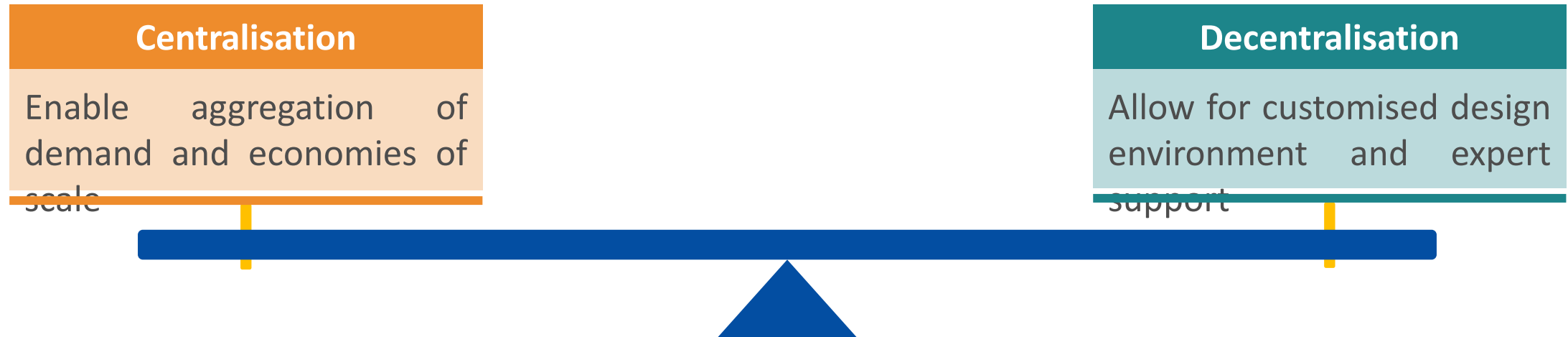
Key considerations for implementation



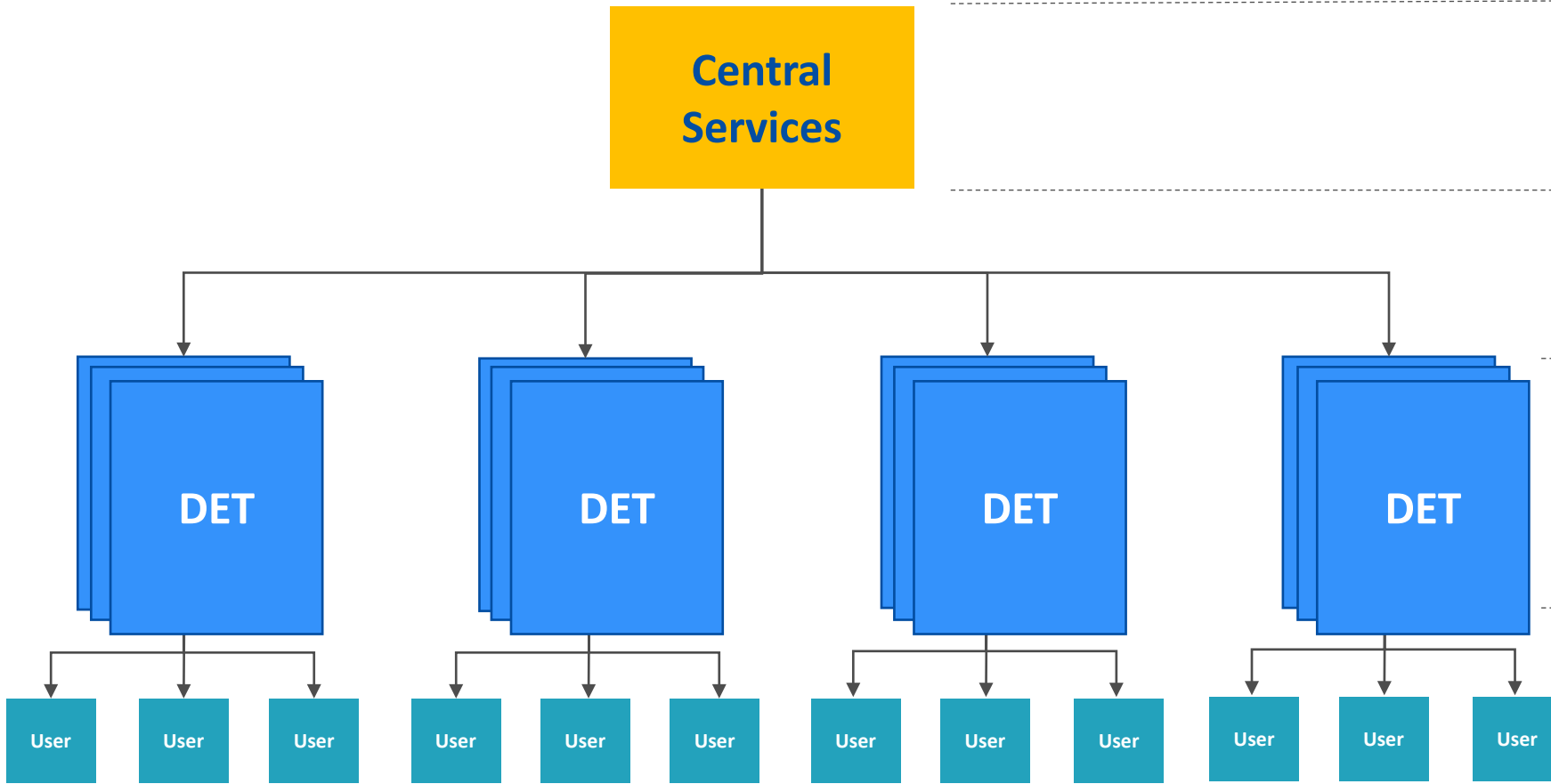
Services to be provided by the Design Platform



Finding the right balance...



Design Platform Architecture



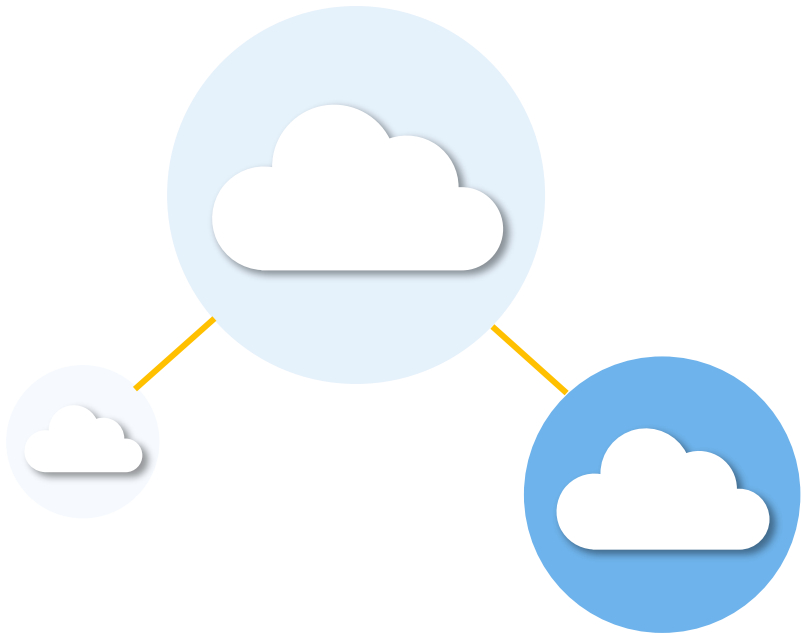
Central services

- Coordination of the Design Platform + link to Chips for Europe Initiative Infrastructure
- Negotiation of framework agreements with vendors
- Hosting of licence server
- Definition of common look and feel across Design Enablement Teams (DETs), quality assurance
- Development of Infrastructure as Code

Distributed services

- Design Enablement Teams** with application engineering support to users
- Hosting of cloud instance
- Supporting users in setting up their design environment and design flows
- Interface with foundries for prototyping
- Supply chain management for prototypes and volume products
- Expert support for validation/characterization and qualification of IP and volume products

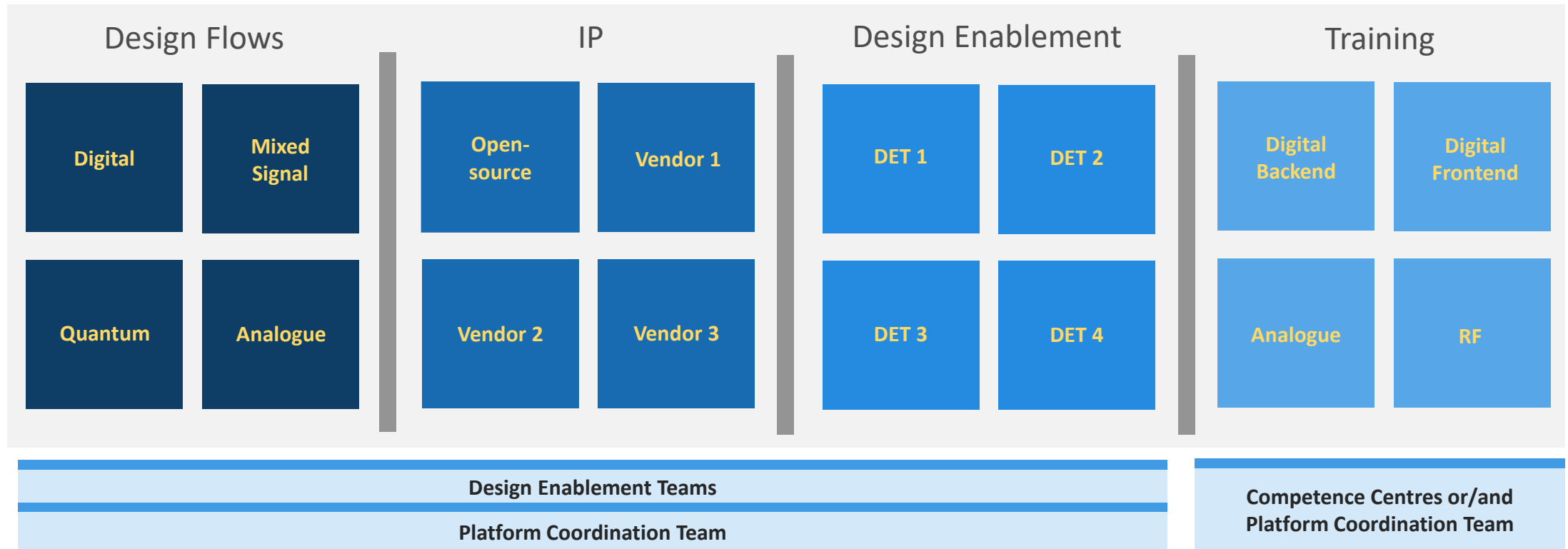
Cloud Implementation



Multi-cloud environment – the platform will be vendor neutral.

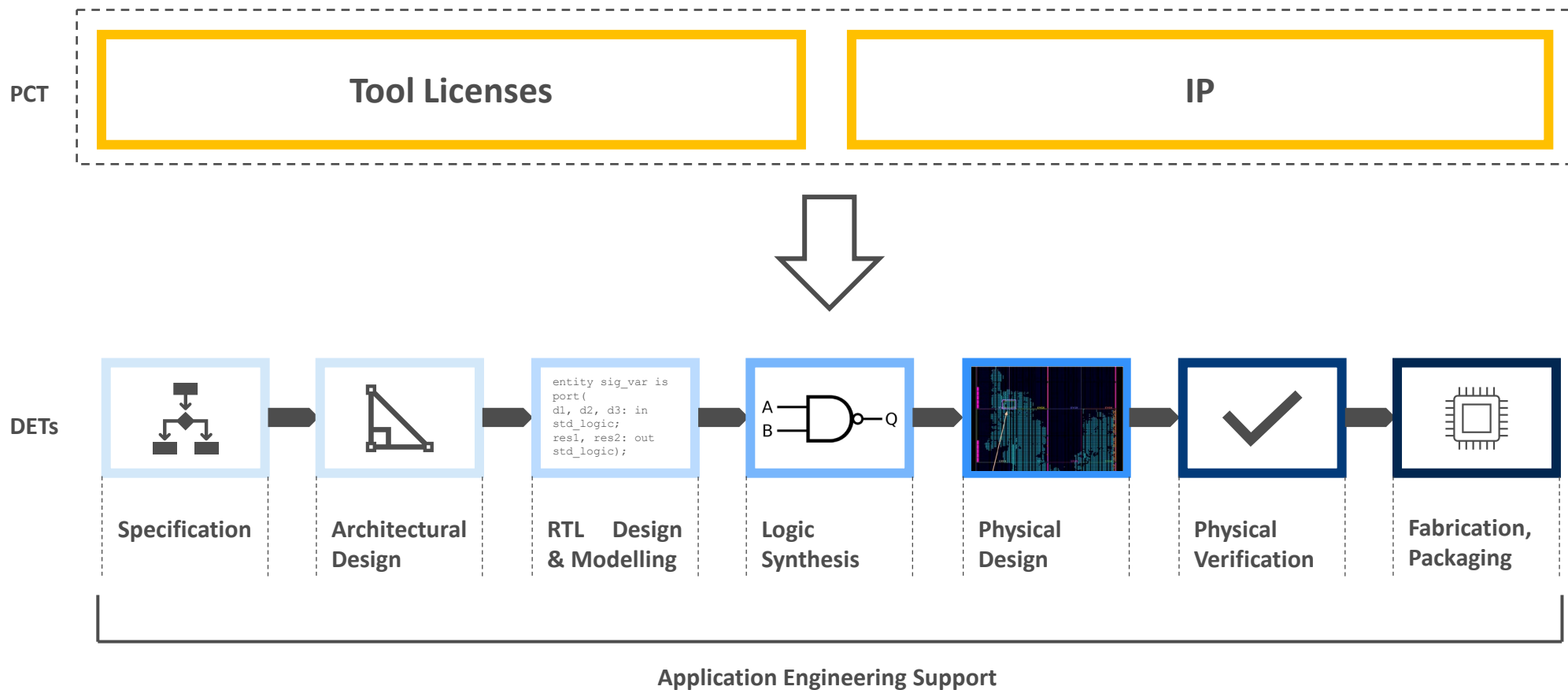
The Platform Coordination Team will be responsible for establishing **framework contracts** with multiple vendors who follow a number of set requirements.

Enabling users through choice



Tiles and options are only examples – eventual implementation may include a different number and type of resources.

Design Platform – Scope of Support





Let's **democratise** access to chip design in
see you in 2024!
Europe

eu-
microelectronics@ec.europa.eu

Why go for a Cloud-based solution?

Rationale

*To provide users with sufficient **scalable** computing resources in an environment that **enables collaboration**. Given the diverse needs of users, the cloud offers a more **flexible** and **efficient** way to manage the entire programme, allowing for seamless adaptation to varying demands (resources, technologies etc.).*

Why would a user need a DET?

Application Engineering Support

Initial **setup** of **design environment and flow** configured for a specific foundry technology, related IPs and EDA tools selected by the platform users with appropriate **cloud access** control and data permissions.

In-project expert support for specific **design flow** tasks to help users in solving blocking issues

Support for project specific EDA tool **issues** (e.g. generation of test cases), or PDK and foundation IP issues

Silicon Flow Support

Support for **back-end design, verification and testing**

Tape-out handling and **interface with the foundries** (aggregators etc.)

Support for **packaging, test, validation,** and qualification tasks